Journal of Circuits, Systems, and Computers Vol. 24, No. 3 (2015) 1550027 (19 pages) © World Scientific Publishing Company DOI: 10.1142/S0218126615500279



Towards a Test Definition Language for Integrated Circuits^{*}

Mohammad Alshayeb^{†,§}, Muhammad E. S. Elrabaa^{†,¶}, Ayman Hroub^{†,∥}, Amran Al-Aghbari^{†,**}, Aiman H. El-Maleh^{†,††} and Abdelhafid Bouhraoua^{†,‡‡}

[†]Information and Department of Information and Computer Science

[‡]Computer Engineering Department, King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia [§]alshayeb@kfupm.edu.sa [¶]elrabaa@kfupm.edu.sa [¶]g200901930@kfupm.edu.sa ^{**}g200902670@kfupm.edu.sa ^{††}aimane@kfupm.edu.sa ^{‡‡}abouh@kfupm.edu.sa

> Received 28 May 2014 Accepted 27 September 2014 Published 10 November 2014

The Standard Test Interface Language (STIL) is the de-facto standard for transferring test data between the test generation environment and the test equipment. STIL's flexibility and extensibility facilitates its use as the sole input language for automatic test-pattern generation (ATPG). However, STIL format is complex and does not provide support for algorithmic interactive testing which necessitate the use of additional programming languages to do that. In this paper, we propose a new Test Definition Language for Integrated Circuits (TDLIC) based on the Extensible Markup Language (XML). TDLIC is a description language for defining tests of digital ICs in a precise and reusable form. The proposed TDLIC provides a common platform for specifying test data as well as complex test procedures. A case study that includes a validation platform is used to show the full capabilities of TDLIC. The validation platform is an FPGA-based system that emulates the automatic test equipment and a prototype IC with four circuits to be tested.

Keywords: Test description language; integrated circuits testing; XML.

*This paper was recommended by Regional Editor Piero Malcovati. Corresponding author.